Electronic Version
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OUT OF THE BOX VERTICAL TRANSISTOR FOR eDRAM ON SOI

Abstract

The present invention provides a vertical memory device formed in a silicon-on-insulator substrate, where a bitline contacting the upper surface of the silicon-on-insulator substrate is electrically connected to the vertical memory device through an upper strap diffusion region formed through a buried oxide layer. The upper strap diffusion region is formed by laterally etching a portion of the buried oxide region to produce a divot, in which doped polysilicon is deposited. The upper strap region diffusion region also provides the source for the vertical transistor of the vertical memory device. The vertical memory device may also be integrated with a support region having logic devices formed atop the silicon-on-insulator substrate.